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2017년 2월 13일 (월)~15일 (수), 강원도 대명비발디파크

● 주관 SK 하이닉스 KSIA 한국반도체산업협회 COSAR 한국반도체연구조합

● 주최 KPS 한국물리학회 The Korean Physical Society, MRS KOREA 한국재료학회 Materials Research Society of Korea, 대한전기학회, IEIE 대한전자공학회 The Institute of Electronics and Information Engineers, IDEC 반도체설계교육센터 IC DESIGN EDUCATION CENTER

● 후원 GWCVB 강원컨벤션뷰로, SAMSUNG, Dongbu HiTek, Lam RESEARCH, ASML, WONIK IPS, DONGJIN SEMICHEM, TEL TOKYO ELECTRON, SYNOPSYS Silicon to Software, EDWARDS, NP NEW POWER PLASMA, NEXTIN Solutions, EXICON, AP시스템(주) Advanced Process Systems Corporation, semi, cadence, Lot vacuum Leader Of Vacuum Technology, IEEE Electron Device Society Korea Chapter, IEEE SSC Seoul Chapter

G. Device & Process Modeling, Simulation and Reliability 분과

2017년 2월 14일 (화), 08:30-10:00
Room C (사파이어, 2층)

[TC1-G] Device Physics and Characterization 1

좌장: 김대환(국민대학교), 조인욱(SK 하이닉스)

TC1-G-1 **08:30-08:45**	**DFT Study on the Clean-Up Mechanism of InGaAs(001) Native Oxides in Atomic Layer Deposition** In Won Yeu[1,2], Cheol Seong Hwang[2,3], and Jung-Hae Choi[1] *[1]Center for Electronic Materials, Korea Institute of Science and Technology,* *[2]Department of Materials Science and Engineering, Seoul National University,* *[3]Inter-University Semiconductor Research Center, Seoul National University*
TC1-G-2 **08:45-09:00**	**Analysis of Hysteresis Characteristic in 3-D NAND Flash Memory Cells** Ho-Jung Kang, Nagyong Choi, Byung-Gook Park, and Jong-Ho Lee *Department of EECS and ISRC, Seoul National University*
TC1-G-3 **09:00-09:15**	**Charge Transport Mechanism and Low-Frequency Noise Properties in High Mobility ZnON Thin-Film Transistors** Chan-Yong Jeong[1], Hee-Joong Kim[1], Dae-Hwan Kim[1], Hyun-Suk Kim[2], Eok Su Kim[3], Tae Sang Kim[3], Joon Seok Park[3], Jong-Baek Seon[3], Kyoung Seok Son[3], Sunhee Lee[3], Seong-Ho Cho[3], Young Soo Park[3], Dae Hwan Kim[4], and Hyuck-In Kwon[1] *[1]School of Electrical and Electronics Engineering, Chung-Ang University, [2]Department of Material Science and Engineering, Chungnam National University, [3]Samsung Advanced Institute of Technology, [4]School of Electrical Engineering, Kookmin University*
TC1-G-4 **09:15-09:30**	**HfO2(Field Effect Passivation Layer)를 적용한 CMOS image sensor의 Dark current 특성 연구** Seon Man Hwang and Yong Hoon Choi *SK Hynix Inc.*
TC1-G-5 **09:30-09:45**	**A Trap Characterization Method for Float Body PMOSFET Using Pulsed Drain Current Transient** Manh-Cuong Nguyen, Hack-Yeon Kim, Jae-Won Choi, Soo-Yeun Han, An Hoang-Thuy Nguyen, Jungyeon Kim, Sang-Woo Kim, Su-Jin Choi, Jong-Kyu Jun, and Rino Choi *Department of Materials Science and Engineering, Inha University*
TC1-G-6 **09:45-10:00**	**Influence of Active Layer Thickness on the Abnormal Output Characteristics in Amorphous In-Ga-Zn-O TFTs under High Current-Flowing Operation** Hye Ri Yu, Jun Tae Jang, Sungju Choi, Hara Kang, Daehyun Ko, Jaeyoung Kim, Geumho Ahn, Jihyun Lee, Sung-Jin Choi, Dong Myong Kim, and Dae Hwan Kim *School of Electrical Engineering, Kookmin University*

DFT study on the clean-up mechanism of InGaAs(001) native oxides in atomic layer deposition

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Due to the outstanding electron transport properties of Ⅲ-Ⅴ compound semiconductors, they are the one of the promising materials for the next-generation semiconductor materials. However, the difficulty of avoiding the exposure of a Ⅲ-Ⅴ surface to oxygen results in the formation of the native oxides with high density of defect states. Recently, it has been reported that the native oxides are reduced during atomic layer deposition (ALD) process of Al_2O_3 dielectric layer on top, which is called clean-up effect. For ALD, there are many precursors of high-k materials, and the clean-up effect depends on types of ligands and metals of the precursors. In order to efficiently screen the various precursors and find appropriate precursors for the Ⅲ-Ⅴ substrates for achieving optimum clean-up effect, computational methods are essential. In this study, the clean-up reaction of InGaAs(001) was studied by density functional theory (DFT) calculations. As a result of oxidation, the surface is essentially covered by their native oxides, such as As_2O_3, Ga_2O_3, and In_2O_3. Using the native oxide models, reduction mechanism of the native oxides was investigated by calculating the reaction free energy during the ALD half-cycle.